REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated April 22, 2004 (U.S. Patent Office Paper No. 2). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

On September 13, 2004, a telephone conference was had with Examiner Im in relation to the Information Disclosure Statements filed on March 4, 2002 and on November 20, 2002, and in relation to consideration of the documents cited in the International Search Report for the corresponding international application. The Examiner indicated that the Information Disclosure Statements filed on March 4, 2002 and on November 20, 2002 were received and would be considered.

As to the documents cited in the International Search Report for the corresponding international application, the Examiner in the September 13, 2004, telephone conference indicated that if they are already filed in the application they would be considered and, if Applicants submitted a Form PTO-1449 identifying such filed documents, consideration would be indicated on such submitted Form PTO-1449. During the phone conference it was noted that the form PCT/DO/EO/903 (371 Acceptance notice) for the above-referenced application indicated that the U.S. Patent Office had received "Copy of references cited in ISR" and "Copy of the International Search Report". The assistance of the Examiner is appreciated.

Also, submitted concurrently herewith is an Information Disclosure Statement and accompanying form PTO-1449 identifying the remaining documents identified in the International Search Report for the corresponding international application that were not identified on forms PTO-1449 for previously filed Information Disclosure Statements. It is respectfully submitted in that the form PCT/DO/EO/903 (371 Acceptance notice) for the above-referenced application indicated that the U.S. Patent Office had received "Copy of references cited in ISR" and "Copy of the International Search Report", copies of such

documents identified on the form PTO-1449 are not required to be submitted. It is understood such documents will be considered, and consideration of such documents will be noted in an Office communication (See MPEP 1893.03(g)) Also, submitted with the concurrently filed Information Disclosure Statement are English Language abstracts for those foreign documents and the cover page of a U.S. Patent that are also identified in the International Search Report for the corresponding international application and on the accompanying form PTO-1449. Also, it is respectfully submitted and believed that no additional fee is required for consideration of the remaining documents identified in the corresponding International Search Report.

Status of the Claims

As outlined above, Claims 1, 2 and 5 through 8 are pending in this application. Claims 3, 4 and 9 through 11 are being canceled without prejudice or disclaimer, and Claims 1, 2 and 5 through 8 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention.

Additional Amendments

The specification and drawings are being amended to correct formal errors and to better disclose and describe the features of the present invention as claimed.

Formal Objections or Rejections

Claim 1, and as understood Claims 2 through 10, were rejected under 35 U.S.C. § 112, second paragraph, for being indefinite. In response, the amendments to Claims 1, 2 and 5 through 8 include amendments that address this rejection under 35 U.S.C. §112. Also, as noted previously, Claims 3, 4 and 9 through 11 have been cancelled without prejudice or disclaimer of their subject matter. Therefore, withdrawal of the 35 U.S.C. §112, second paragraph, rejection of Claims 1 and 2 through 10 is respectfully requested.

Prior Art Rejections

Claim 1 was rejected under 35 U.S.C. §103(a) over Oyama, JP 10-12809 (Oyama '809) in view of Yoshikawa, U.S. Patent No. 6,199,150 (the Yoshikawa '150 Patent). This rejection is respectfully traversed.

Claims 3, 4 and 7 were rejected under 35 U.S.C. §103(a) over Oyama '809 in view of Smits et al., U.S. Patent No. 5,432,913 (the Smits '913 Patent). As to Claim 7, this rejection is respectfully traversed.

As to the rejection of Claims 3 and 4 under 35 U.S.C. §103(a) over Oyama '809 in view of the Smits '913 Patent, Claims 3 and 4 have been cancelled without prejudice or disclaimer of their subject matter. Therefore, withdrawal of the 35 U.S.C. §103(a) rejection of Claims 3 and 4 is respectfully requested.

Claims 8 through 10 were rejected under 35 U.S.C. §103(a) over Oyama '809 in view of Sato, U.S. Patent No. 5,729,764 (the Sato '764 Patent). As to Claim 8, this rejection is respectfully traversed.

As to the rejection of Claims 9 and 10 under 35 U.S.C. §103(a) over Oyama '809 in view of the Sato '764 Patent, Claims 9 and 10 have been cancelled without prejudice or disclaimer of their subject matter. Therefore, withdrawal of the 35 U.S.C. §103(a) rejection of Claims 9 and 10 is respectfully requested.

Claims 5 and 6 were rejected under 35 U.S.C. §103(a) over Oyama '809 in view of the Smits '913 Patent and Takemae et al., U.S. Patent No. 6,078,514 (the Takemae '514 Patent). This rejection is respectfully traversed.

Claim 2 was rejected under 35 U.S.C. §103(a) over Oyama '809 and the Yoshikawa '150 Patent, as applied to Claim 1, and further in view of the Takemae '514 Patent. This rejection is respectfully traversed.

Claim 11 was rejected under 35 U.S.C. §103(a) over Oyama '809 in view of the Smits '913 Patent, as applied to Claim 8, and further in view of the Takemae '514 Patent. Claim 11

has been cancelled without prejudice or disclaimer of its subject matter. Therefore, withdrawal of the 35 U.S.C. §103(a) rejection of Claim 11 is respectfully requested.

The above rejections of the presently pending Claims 1, 2, and 5 through 8 will be considered collectively and individually.

Discussion as to the Rejection of Claim 1

As to the rejection of independent Claim 1 over Oyama '809 in view of the Yoshikawa '150 Patent, Oyama '809 discloses a plurality of electronic components 21 and 22 and a wiring substrate 1 wherein a first wiring line 10 connects an external input-output signal conductive pad 5 with the terminals of the electronic components 21 and 22 and a second wiring line 11 connects between the terminals of the electronic components 21 and 22, with the second wiring line connected to an inspection conductive pad 4. (Abstract of Oyama '809).

Further, Oyama '809 does not disclose a relation to determine placement of electrodes (such as external connecting electrodes 15sg, 15vs, 15da, 15db in the above-referenced application) by placement of electronic parts (such as semiconductor integrated circuit chips 11, 12, 13, 14 in the above-referenced application) disposed on a wiring board (such as module substrate 10 in the above-referenced application) in relation to the operation speed of the electronic parts.

In addition, the Yoshikawa '150 Patent discloses forming on a data storage unit 100 connections of memory devices of different transmission speeds to separate buses. However, the Yoshikawa '150 Patent does not disclose determining of placement of electrodes by placement of electronic parts disposed on a wiring board in relation to the operation speed of the electronic parts.

Therefore, it is respectfully submitted that Oyama '809 and the Yoshikawa '150 Patent do not disclose a multichip module including a module substrate having plural wiring layers, a plurality of external connecting electrodes formed on one face of the module substrate, and a plurality of mounting pads for mounting a plurality of semiconductor

integrated circuit chips formed on the other face of the module substrate, wherein the area for the mounting pad for semiconductor integrated circuit chips operated at relatively low speed on the front face of the module substrate is coupled to the external connecting electrodes of the plurality of external connecting electrodes for the address outputs and the data inputs-outputs operated at relatively low speed, as respectively recited in independent Claim 1.

Discussion as to the Rejection of Claim 7

As to the rejection of Claim 7 under 35 U.S.C. §103(a) over Oyama '809 in view of the Smits '913 Patent, as stated previously, Oyama '809 discloses a plurality of electronic components 21 and 22 and a wiring substrate 1 wherein a first wiring line 10 connects an external input-output signal conductive pad 5 with the terminals of the electronic components 21 and 22 and a second wiring line 11 connects between the terminals of the electronic components 21 and 22, with the second wiring line connected to an inspection conductive pad 4. (Abstract of Oyama '809).

Further, the Smits '913 Patent discloses in relation to Figure 4C therein a sandwiched board (PCB board 404) on which are disposed memories (SRAMs 126).

However, it is respectfully submitted that Oyama '809 and the Smits '913 Patent do not disclose a semiconductor module in which a plurality of external connecting electrodes are arranged on one face of a module substrate and a mounting pattern is formed on the other face of the module substrate, wherein the mounting pattern and the plurality of external connecting electrodes are electroconductively coupled to each other through an anisotropic electroconductive film, with each grouped pattern for arranging semiconductor integrated circuit chips of the same kind in a group being electroconductively coupled to the plurality of external connecting electrodes through a corresponding anisotropic electroconductive film, as respectively recited in independent Claim 7.

Discussion as to the Rejection of Claim 8

As to the rejection of Claim 8 under 35 U.S.C. §103(a) over Oyama '809 in view of the Sato '764 Patent, Oyama '809 does not disclose determining of placement of electrodes by placement of electronic parts disposed on a wiring board, as respectively recited in Claim 8. Oyama '809 discloses a plurality of electronic components 21 and 22 and a wiring substrate 1 wherein a first wiring line 10 connects an external input-output signal conductive pad 5 with the terminals of the electronic components 21 and 22 and a second wiring line 11 connects between the terminals of the electronic components 21 and 22, with the second wiring line connected to an inspection conductive pad 4. (Abstract of Oyama '809).

Further, the Sato '764 Patent discloses a bus interface circuit of an integrated circuit and an input/output buffer circuit and does not disclose determining of placement of electrodes by placement of electronic parts disposed on a wiring board, as respectively recited in Claim 8.

Therefore, Oyama '809 and the Sato '764 Patent do not disclose an electronic circuit including a first semiconductor device and a second semiconductor device, with the second semiconductor device for operation at a relatively high speed in comparison with the operation speed of the first semiconductor device, and wherein the first semiconductor device and the second semiconductor device are mounted to a bus of a multilayer wiring substrate in a common connecting state; wherein the second semiconductor device has a data processor chip and a memory chip commonly connected to the bus through a plurality of external connecting electrodes in the multilayer wiring substrate, and wherein external connecting electrodes of the plurality of external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of the multilayer wiring substrate corresponding to an area on the front face of the multilayer wiring substrate for mounting the memory chip, as respectively recited in independent Claim 8.

Discussion as to the Rejection of Claims 5 and 6

As to the rejection of Claims 5 and 6 under 35 U.S.C. §103(a) over Oyama '809 in view of the Smits '913 Patent and the Takemae '514 Patent, as previously stated, Oyama '809 discloses a plurality of electronic components 21 and 22 and a wiring substrate 1 wherein a first wiring line 10 connects an external input-output signal conductive pad 5 with the terminals of the electronic components 21 and 22 and a second wiring line 11 connects between the terminals of the electronic components 21 and 22, with the second wiring line connected to an inspection conductive pad 4. (Abstract of Oyama '809).

Further, as discussed previously, the Smits '913 Patent discloses in relation to Figure 4C therein a sandwiched board (PCB board 404) on which are disposed memories (SRAMs 126).

However, Oyama '809 and the Smits '913 Patent do not disclose determining of placement of electrodes by placement of electronic parts disposed on a wiring board, as respectively recited in Claims 5 and 6.

Moreover, the Takemae '514 Patent discloses a semiconductor device and semiconductor system that includes at least one logic chip and at least one memory chip arranged such that one side of the at least one memory chip faces one side of the at least one logic chip (Abstract, Takemae '514 Patent). Also, the Takemae '514 Patent discloses power-voltage nodes situated on the one side of the logic chip and power voltage nodes situated on the one side of the memory chip, with power voltage lines arranged between the logic chip and the memory chip. (Col. 20, lines 13-58). The Takemae '514 Patent further discloses that the power supply pads 23 of the plural chips are disposed in a semiconductor system including memory chip 12 and logic chip 11 in a same package 10 in a side to side opposed relation. (Figure 5 of the Takemae '514 Patent).

However, while the Takemae '514 Patent discloses power-voltage nodes situated to one side of the memory chip and to one side of the logic chip and the power supply pads 23, the Takemae '514 Patent does not disclose determining of placement of electrodes by

placement of electronic parts disposed on a wiring board, as respectively recited in Claims 5 and 6.

Therefore, Oyama '809, the Smits '913 Patent and the Takemae '514 Patent do not disclose a multichip module including a module substrate having a plurality of wiring layers, a plurality of external connecting electrodes formed on one face of the module substrate, a mounting pad formed on the other face of the module substrate, and a data processor chip, a memory chip and a buffer circuit arranged on the module substrate through the mounting pad, wherein external connecting electrodes of the plurality of external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of the module substrate corresponding to an area on the front face of the module substrate for mounting the memory chip, as respectively recited in independent Claim 5.

Moreover, Oyama '809, the Smits '913 Patent and the Takemae '514 Patent do not disclose a multichip module including a module substrate having a plurality of wiring layers, a plurality of external connecting electrodes formed on one face of the module substrate, a mounting pad formed on the other face of the module substrate, and a plurality of kinds of semiconductor integrated circuit chips mounted through the mounting pad on the front face of the module substrate, wherein external connecting electrodes of the plurality of external connecting electrodes for operating power allocated to supply a power voltage and a ground voltage are partly coarsely and partly closely arranged on the module substrate, and are closely arranged to the rear faces of the semiconductor integrated circuit chips of the plurality of kinds of semiconductor integrated circuit chips having larger power consumption, as respectively recited in independent Claim 6.

Discussion as to the Rejection of Claim 2

As to the rejection of Claim 2 under 35 U.S.C. §103(a) over Oyama '809 in view of the Yoshikawa '150 Patent, as applied to Claim 1, and further in view of the Takemae '514 Patent, as previously mentioned, Oyama '809 and the Yoshikawa '150 Patent do not disclose

a relation to determine placement of electrodes by placement of electronic parts disposed on a wiring board in relation to the operation speed of the electronic parts.

Also, as previously mentioned, while the Takemae '514 Patent discloses power-voltage nodes situated to one side of the memory chip and to one side of the logic chip and the power supply pads 23, the Takemae '514 Patent similarly does not disclose a relation to determine placement of electrodes by placement of electronic parts disposed on a wiring board in relation to the operation speed of the electronic parts.

Therefore, Oyama '809, the Yoshikawa '150 Patent and the Takemae '514 Patent do not disclose a multichip module, wherein external connecting electrodes of the plurality of external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on the rear face of the module substrate corresponding to the area for the mounting pad for semiconductor integrated circuit chips operated at relatively high speed on the front face of the module substrate for mounting the semiconductor integrated circuit chips operated at relatively high speed, as respectively recited in dependent Claim 2.

Conclusion

In view of the foregoing, it is respectfully submitted that the claimed subject matter of Claims 1, 2 and 5 through 8 is not obvious over Oyama '809, the Smits '913 Patent, the Yoshikawa '150 Patent, the Takemae '514 Patent and the Sato '764 Patent, as respectively applied in the above rejections of these claims. Also, as previously mentioned, Claims 3, 4 and 9 through 11 have been cancelled without prejudice or disclaimer of their subject matter. Wherefore, withdrawal of the 35 U.S.C. §103(a) rejections of Claims 1 through 11 is respectfully requested.

Reconsideration and allowance of Claims 1, 2 and 5 through 8 are respectfully requested.

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office action rely. These differences are more

than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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September 22, 2004

IN THE DRAWINGS

Please approve the changes to the drawings as outlined in the attached Letter to the Office Draftsperson, and as shown in the accompanying revised replacement drawings for Figures 6, 8 and 17. Specifically, Figure 6 has been corrected to include the numeral 28D, Figure 8 has been corrected as to designation for the numerals 21A and 21B and spelling, and Figure 17 has been corrected to include the numeral 28D.